



A Simple Low Cost Speed Log Interface for Oceanographic Data Acquisition System

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Abstract

A speed log interface is designed with parallel Binary Coded Decimal output. This design was mainly required for the oceanographic data acquisition system as an interface between the speed log and the computer. However, this can also be used as a low cost stand alone speed log along with a simple outboard rotor type sensor.

Introduction

Ship's speed is an important information required on board research vessels as well as survey vessels for navigational purposes. Satellite navigation systems use this information to calculate the ship's position during dead reckoning period. Ship's speed log do not provide BCD outputs which need to be interfaced to the oceanographic data acquisition system. Fishing trawlers which are generally chartered for near shore surveys do not have a speed log. In this paper we have proposed a circuit for a speed display using a simple rotor type outboard speed sensor. The parallel BCD(Binary Coded Decimal) output provided can be interfaced to a oceanographic data acquisition system. Displays are provided for a visual read-out. This equipment can also be used as a stand alone speed log.

Block Diagram

The design is simple and is with minimum possible components and is fairly accurate. The speed information is normally acquired from an outboard rotor type sensor towed by its own cable. It provides a standard 200 pulses per nautical mile, contact closures. It can also be used as a repeater to a doppler or an electromagnetic speed log normally available on large vessels. The design has a flexibility of selecting three types of inputs, viz. contact closure, standard 5 volt TTL and RS 232 level. The block diagram is shown in Fig. 1. The speed information from the rotor sensor is fed to a signal conditioner. It raises the signal level to TTL level. The gate allows the pulses to pass through it for a predetermined time width. This width is provided by a timing control circuit. The timing control circuit comprises of a clock generator and a divider network. It provides accurate timing set by the timing control and is fed to latching circuit. The latching circuit gets the speed information from the counters and the latching pulse is acquired from the timing control. The BCD outputs from the latches are fed to the decoder/drivers which in turn drive seven segment displays. BCD output is also brought out through buffers for use by oceanographic data acquisition system.

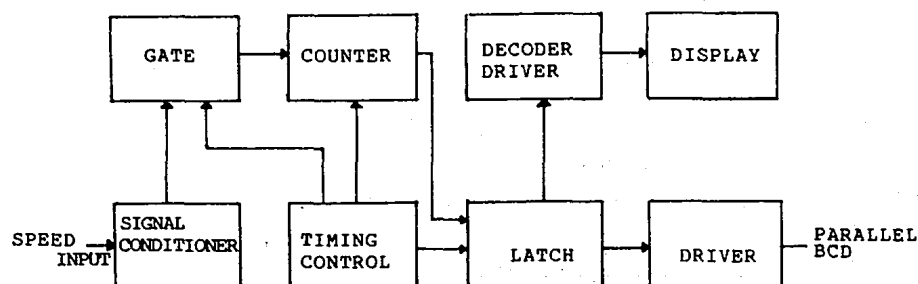


Fig.1: Block Diagram

Circuit Description

The schematic diagram is shown in Fig 2. A stable 60 Hz clock is generated by a Quartz crystal driven oscillator/divider

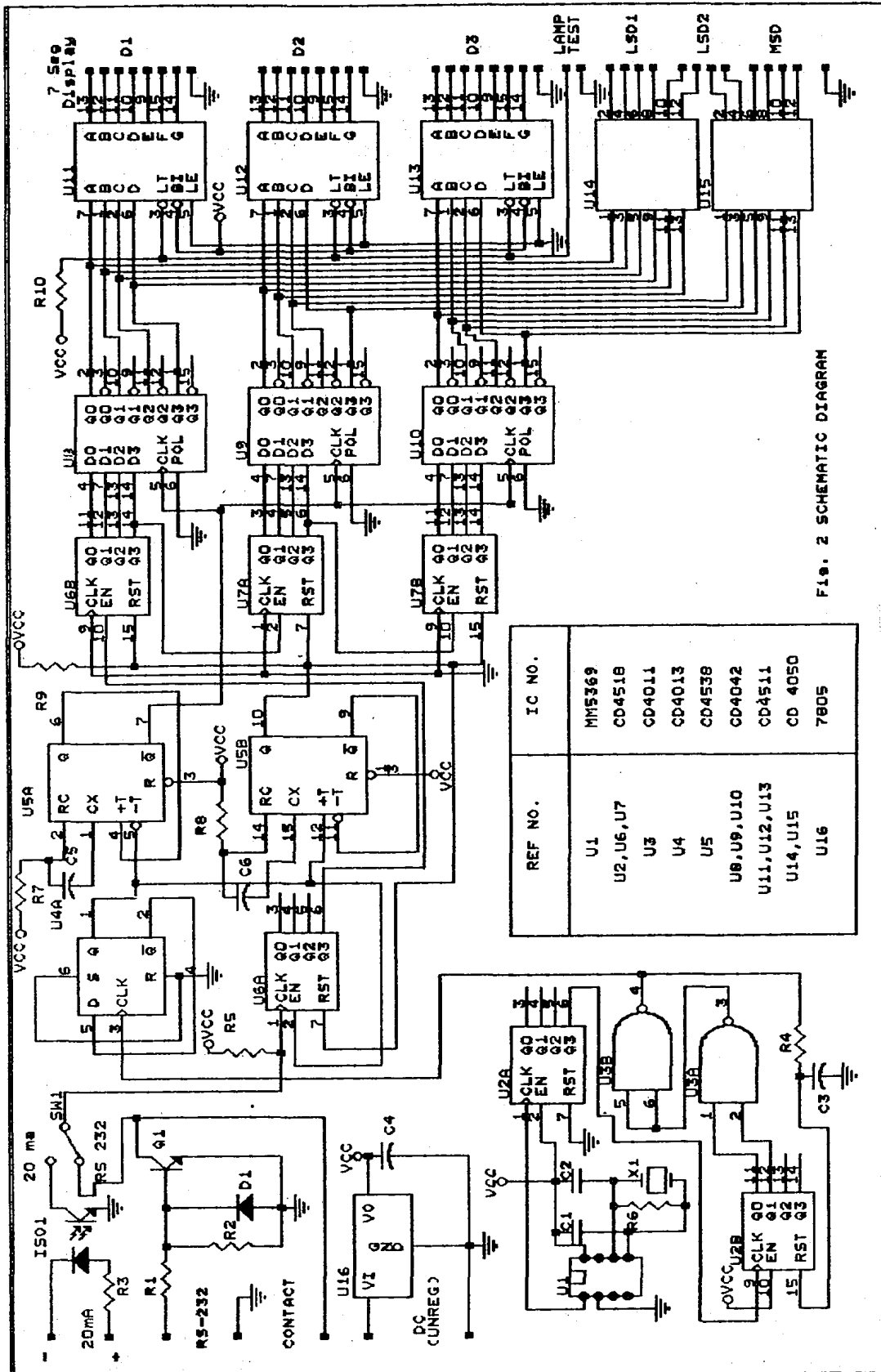


FIG. 2 SCHEMATIC DIAGRAM

REF NO.	IC NO.
U1	MM5369
U2,U6,U7	CD4518
U3	CD4011
U4	CD4013
U5	CD4538
U8,U9,U10	CD4042
U11,U12,U13	CD4511
U14,U15	CD 4050
U16	7805

U1. This is then divided by counters U2A and U2B along with NAND gates U3A and U3B to produce 2 Hz. A D flip flop U4A converts this 2 Hz clock to 1 Hz clock with equal mark to space ratio. This 1 Hz clock triggers the monostables U5A and U5B for latching and resetting the counters and is also fed to counter enable input.

The switch SW_1 selects the type of input for the speed information. 20 mA input is isolated by an opto isolator. Transistor Q_1 acts as a level converter for RS 232 and diode D_1 prevents negative portions. The 5 volt TTL level is achieved by a pull up resistor R_5 for contact closure as well as RS 232 level. The speed pulses are fed to the counter U6A. This counter is gated by a 500 m sec. gating pulse from Q output of U4A. Thus the number of pulses for a period of 500 m sec. are counted. The counter U6A forms second decimal count of the speed. The counters U6B, U7A and U7B are cascaded along with U6A to get the required count. The monostable U5A provides the latching pulse to all the three latches after the gating is over. During the 500 m sec. low state of the clock, the monostable U5B resets all the counters everytime. The latched data is recorded by U11, U12 and U13 and fed to 7 segment displays. This data is also buffered by U14, U15 and is available at the BCD output socket. The circuit is powered by 5 volt provided through regulator U15.

Application

This circuit was mainly designed for speed display and as an interface to an oceanographic data acquisition system. It can also be used as a stand alone low cost speed log for small vessels. It is also useful for near shore oceanographic surveys. For deep sea applications, it is useful as a repeater for doppler and electromagnetic speed logs.

Future Modifications

The design discussed above counts the pulses in asynchronous mode. However, a synchronizing circuit can be added so that the gate will synchronize with the incoming pulses. This will improve the accuracy of this design. The optional facilities like distance travelled and alarm facilities for speed limits can also be incorporated.

Acknowledgement

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